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EXAMINER	
TORRES, JUAN A	

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2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,585	MCDONOUGH ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9 and 11-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 11-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

The modifications to the claims were received on 08/05/2006. These modifications are accepted by the Examiner.

In view of the amendment filed on 08/05/2006, the Examiner withdraws the claims objections to claim 20 of the previous Office action.

Response to Arguments

Applicant's arguments filed on 08/05/2006 have been fully considered but they are not persuasive.

Regarding claims 15-22:

The Applicant contends, "Examiner has rejected depending claim 16, which also recites thee memory of independent claim 15. Examiner identifies figures 6-9 and column 8, line 11 through column 10, line 23 of Stark et al. as anticipatory disclosure for claim 16. Applicants respectfully disagree. Stark et al. disclose a shift register at Figure 4 which iteratively produces each sequence as needed. Operation of this shift register is explained at column 7, line 42 through column 8, line 35. Applicants fail to find any disclosure by Stark et al. of "a memory arranged to store a plurality of phase-shifting masks at a first time" as required by claims 15-22. Thus, applicants respectfully submit that claims 15-22 are patentable under 35 U.S.C. § 102(e) over Stark et al.".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Stark specifically discloses in column 10 lines 52-61 "memory means for storing combining information that corresponds to pre-determined sleep intervals; means for

extracting particular combining information from said memory means in response to said control information; and means for applying said combining information to selectively combine elements of said extracted current operating state using combinatorial logic to determine said new operating state" (emphasis added), and also in column 8 lines 11-54 "If only one shift or multiples of it are needed, then the matrix is fixed and the corresponding combining logic can be used without the need for a matrix input, as shown in FIG. 4. The example in FIG. 4 provides a fixed shift of ten steps. However, circuitry for a shift having an arbitrary number of steps may also be beneficial, e.g., to compensate for awaking after different duration sleep periods. In order to calculate an arbitrary shift, an arbitrary power of M needs to be computed. If N is the length of the shift register sequence, e.g., N=31, any power of M up to 30 can be computed by multiplying some of the following: M M^2 M^4 M^8 M^{16} For example, to obtain M^{10}, $M^8 * M^2$ is calculated. If a particular shift of the nominal sequence is currently being used and an additional shift is desired, then multiplying the current M by another power of M will provide a new shift. This can be accomplished using mod-N arithmetic of the two shifts to obtain a new binary representation of the desired shift. To obtain different shifts requires different connections in the combining logic. An arbitrary shift can be obtained by having five different shifting operations that are either gated on or off as shown in FIG. 6. Therein, shift register generator 60 holds the current or "old" sequence state. The first circuit 62 forms a shift of this sequence by one clock cycle. The second circuit 64 takes the output of circuit 62 and shifts it by two clock cycles. The third circuit 66 shifts the output of circuit 64 by four clock cycles. The fourth circuit 68 shifts the

output of circuit 66 by 8 clock cycles and the last stage 69 shifts the output of circuit 68 by 16 cycles. By selectively gating each of these circuits, i.e., to either include their contribution or not, an arbitrary shift is obtained. In FIG. 6 the lines labeled b_1, b_2, . . . b_{16} are the bits in the binary representation of the desired shift. At each block 62-69 the input is either multiplied by M^j or not multiplied depending on whether the corresponding gating bit b is 1 or zero, respectively. For example, to shift the current sequence contained in SRG 60 by 13 steps into the future, bits b_1 -b_{16} would be set as follows: b_1 =1, b_2 =0, b_4 =1, b_8 =1, b_{16} =0" (emphasis added).

For these reasons and the reasons indicated in the previous Office action the rejection of claims 15-22 are maintained.

Regarding claims 1-2, 4-9, 11-14 and 23-25:

The Applicant contends, "Stark et al. do not disclose Stark discloses selecting a plurality of phase-shifting masks stored in a memory at a first time in response to a first time interval" as required by claims 1-2, 4-9 and 11-14. Furthermore, Stark et al. do not disclose "selecting a plurality of phase-shifting masks stored in a memory at a first time" as required by claim 25".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, The Examiner disagrees and asserts, that, as indicated in the previous Office action, Stark specifically discloses in column 10 lines 52-61 "memory means for storing combining information that corresponds to pre-determined sleep intervals; means for extracting particular combining information from said memory means in response to said control information; and means for applying said combining information

to selectively combine elements of said extracted current operating state using combinatorial logic to determine said new operating state" (emphasis added), and also in column 8 lines 11-54 "If only one shift or multiples of it are needed, then the matrix is fixed and the corresponding combining logic can be used without the need for a matrix input, as shown in FIG. 4. The example in FIG. 4 provides a fixed shift of ten steps. However, circuitry for a shift having an arbitrary number of steps may also be beneficial, e.g., to compensate for awaking after different duration sleep periods. In order to calculate an arbitrary shift, an arbitrary power of M needs to be computed. If N is the length of the shift register sequence, e.g., N=31, any power of M up to 30 can be computed by multiplying some of the following: M M^2 M^4 M^8 M^{16} For example, to obtain M^{10}, M^8 * M^2 is calculated. If a particular shift of the nominal sequence is currently being used and an additional shift is desired, then multiplying the current M by another power of M will provide a new shift. This can be accomplished using mod-N arithmetic of the two shifts to obtain a new binary representation of the desired shift. To obtain different shifts requires different connections in the combining logic. An arbitrary shift can be obtained by having five different shifting operations that are either gated on or off as shown in FIG. 6. Therein, shift register generator 60 holds the current or "old" sequence state. The first circuit 62 forms a shift of this sequence by one clock cycle. The second circuit 64 takes the output of circuit 62 and shifts it by two clock cycles. The third circuit 66 shifts the output of circuit 64 by four clock cycles. The fourth circuit 68 shifts the output of circuit 66 by 8 clock cycles and the last stage 69 shifts the output of circuit 68 by 16 cycles. By selectively gating each of these circuits, i.e., to either include their

contribution or not, an arbitrary shift is obtained. In FIG. 6 the lines labeled b_1, b_2, . . . b_{16} are the bits in the binary representation of the desired shift. At each block 62-69 the input is either multiplied by M^j or not multiplied depending on whether the corresponding gating bit b is 1 or zero, respectively. For example, to shift the current sequence contained in SRG 60 by 13 steps into the future, bits b_1 -b_{16} would be set as follows: b_1 =1, b_2 =0, b_4 =1, b_8 =1, b_{16} =0" (emphasis added).

For these reasons and the reasons indicated in the previous Office action the rejection of claims 1-2, 4-9, 11-14 and 23-25 are maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Stark (US 6282181 B1).

As per claim 15, Stark discloses a memory arranged to store a plurality of phase-shifting masks at a first time (column 10 lines 52-53; column 11 lines 23-24); a memory port to supply the plurality of phase-shifting masks (column 10 lines 55-57. Stark specifically discloses in column 10 lines 52-61 "memory means for storing combining information that corresponds to pre-determined sleep intervals; means for extracting

particular combining information from said memory means in response to said control information; and means for applying said combining information to selectively combine elements of said extracted current operating state using combinatorial logic to determine said new operating state" (emphasis added), and also in column 8 lines 11-54 "If only one shift or multiples of it are needed, then the matrix is fixed and the corresponding combining logic can be used without the need for a matrix input, as shown in FIG. 4. The example in FIG. 4 provides a fixed shift of ten steps. However, circuitry for a shift having an arbitrary number of steps may also be beneficial, e.g., to compensate for awaking after different duration sleep periods. In order to calculate an arbitrary shift, an arbitrary power of M needs to be computed. If N is the length of the shift register sequence, e.g., N=31, any power of M up to 30 can be computed by multiplying some of the following: M M^2 M^4 M^8 M^{16} For example, to obtain M^{10}, $M^8 * M^2$ is calculated. If a particular shift of the nominal sequence is currently being used and an additional shift is desired, then multiplying the current M by another power of M will provide a new shift. This can be accomplished using mod-N arithmetic of the two shifts to obtain a new binary representation of the desired shift. To obtain different shifts requires different connections in the combining logic. An arbitrary shift can be obtained by having five different shifting operations that are either gated on or off as shown in FIG. 6. Therein, shift register generator 60 holds the current or "old" sequence state. The first circuit 62 forms a shift of this sequence by one clock cycle. The second circuit 64 takes the output of circuit 62 and shifts it by two clock cycles. The third circuit 66 shifts the output of circuit 64 by four clock cycles. The fourth circuit 68 shifts the output

of circuit 66 by 8 clock cycles and the last stage 69 shifts the output of circuit 68 by 16 cycles. By selectively gating each of these circuits, i.e., to either include their contribution or not, an arbitrary shift is obtained. In FIG. 6 the lines labeled b_1, b_2, . . . b_{16} are the bits in the binary representation of the desired shift. At each block 62-69 the input is either multiplied by M^j or not multiplied depending on whether the corresponding gating bit b is 1 or zero, respectively. For example, to shift the current sequence contained in SRG 60 by 13 steps into the future, bits b_1 -b_{16} would be set as follows: b_1 =1, b_2 =0, b_4 =1, b_8 =1, b_{16} =0" (emphasis added)); an application means to determine a first time interval, the application means cross-referencing the first time interval to the plurality of phase-shifting masks, the application means having an output connected to the memory port to request the plurality of phase-shifting masks (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61); and a pseudorandom noise (PN) code generator having a first input connected to the memory to accept the plurality of phase-shifting masks, the PN code generator offsetting a PN code with each phase-shifting mask of the plurality of phase-shifting masks, the PN code generator having an output to supply the PN code with a second phase, offset from the PN code first phase (figure 1 block 320, figures 6-9 column 8 line 11 to column 10 line 23. The have to use each of the shifting masks because the final shift is obtained only using all the masks selected to produce the shift).

As per claim 16, Stark discloses claim 15, Stark also discloses that the memory includes a plurality of phase-shifting masks (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61); and wherein the application means cross-references a

plurality of time intervals to the plurality of phase-shifting masks the memory (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61).

As per claim 17, Stark discloses claim 16, Stark also discloses that the PN code generator generates the PN code at a first chip period (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 30-31); wherein the application means determines a first time interval proportionally related to the first chip period (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 58-61); and wherein the memory supplies a phase-shifting mask that is offset by a PN code phase shift proportionally related to the first time interval (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-57).

As per claim 18, Stark discloses claim 17, Stark also discloses that the PN code has $(2^N - 1)$ states with a period m= $(2^N - 1)$ time the first chip period (column 1 lines 21-40); the application means determines a first time interval from the plurality of first time intervals in the range between zero and m, with a resolution of x (figures 6-9 column 8 line 11 to column 10 line 23.); and generating a PN code with a second phase that is offset with respect to time in units of x (figures 6-9 column 8 line 11 to column 10 line 23. The final shift is obtained only using all the masks selected to produce the shift).

As per claim 19, Stark discloses claim 18, Stark also discloses that x is equal to the first chip period (column 8 lines 11-54).

As per claim 20, Stark discloses claim 18, Stark also discloses a sleep clock having an output connected to the application means with a period of q times the first chip period, where q is an integer (figures 6-9 column 8 line 11 to column 10 line 23;

column 10 lines 26-42); and wherein the application means includes a plurality of time intervals having a resolution of x equal to the sleep clock period (figures 6-9 column 8 line 11 to column 10 line 23).

As per claim 21, Stark discloses claim 18, Stark also discloses that the application means includes a plurality of first time intervals in the range between x and nx (figures 6-9 column 8 line 11 to column 10 line 23); and the memory includes n phase shift masks corresponding to the plurality of first time periods between x and nx (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61).

As per claim 22, Stark discloses claim 18, Stark also discloses that the application means includes a plurality of time intervals in the range between x and nx (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61); wherein the application means selects a plurality of $\log_2$ (n) time intervals to form a first interval sum (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61); wherein the memory includes $\log_2$ (n) phase-shifting masks corresponding to $\log_2$ (nx) intermediate time intervals between x and nx (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61); and wherein the application means selects a plurality of phase-shifting masks from the memory corresponding to a plurality of time intervals in the first time interval sum (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61); wherein the memory supplies the selected phase-shifting masks to the PN code generator (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61); and wherein the PN code generator iteratively shifts the PN code first phase with each

of the plurality of selected phase-shifting masks to supply the PN code second phase (figures 6-9 column 8 line 11 to column 10 line 23; column 10 lines 52-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-9, 11-14 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easton (US 6590886) in view of Stark (US 6282181 B1).

As per claim 1, Easton discloses a method for shifting the phase of a pseudorandom noise (PN) code comprising accepting a PN code with a first phase (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64); determining a first time interval (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64; the first time interval is the time reference provided by the searcher 205); selecting a phase-shifting mask in response to the first time interval (figure 1 block 207A-207N column 4 lines 53-56); shifting the PN code first phase with the phase-shifting mask from a plurality of selected phase-shifting masks (figure 1 block 207A-207N column 4 lines 37-64; and column 8 lines 45-64 indicates how the shifting is done using the mask); and generating a PN code with a second phase, offset by the first time interval from the PN code first phase (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64). Easton

doesn't disclose selecting a plurality of phase-shifting masks stored in a memory at a first time in response to a first time interval; and shifting the PN code first phase with each of the phase-shifting mask. Stark discloses selecting a plurality of phase-shifting masks stored in a memory at a first time in response to a first time interval (column 10 lines 52-61 "memory means for storing combining information that corresponds to pre-determined sleep intervals; means for extracting particular combining information from said memory means in response to said control information; and means for applying said combining information to selectively combine elements of said extracted current operating state using combinatorial logic to determine said new operating state" (emphasis added), and also in column 8 lines 11-54 "If only one shift or multiples of it are needed, then the matrix is fixed and the corresponding combining logic can be used without the need for a matrix input, as shown in FIG. 4. The example in FIG. 4 provides a fixed shift of ten steps. However, circuitry for a shift having an arbitrary number of steps may also be beneficial, e.g., to compensate for awaking after different duration sleep periods. In order to calculate an arbitrary shift, an arbitrary power of M needs to be computed. If N is the length of the shift register sequence, e.g., N=31, any power of M up to 30 can be computed by multiplying some of the following: M M^2 M^4 M^8 M^{16} For example, to obtain M^{10}, M^8 * M^2 is calculated. If a particular shift of the nominal sequence is currently being used and an additional shift is desired, then multiplying the current M by another power of M will provide a new shift. This can be accomplished using mod-N arithmetic of the two shifts to obtain a new binary representation of the desired shift. To obtain different shifts requires different connections in the combining

logic. An arbitrary shift can be obtained by having five different shifting operations that are either gated on or off as shown in FIG. 6. Therein, shift register generator 60 holds the current or "old" sequence state. The first circuit 62 forms a shift of this sequence by one clock cycle. The second circuit 64 takes the output of circuit 62 and shifts it by two clock cycles. The third circuit 66 shifts the output of circuit 64 by four clock cycles. The fourth circuit 68 shifts the output of circuit 66 by 8 clock cycles and the last stage 69 shifts the output of circuit 68 by 16 cycles. By selectively gating each of these circuits, i.e., to either include their contribution or not, an arbitrary shift is obtained. In FIG. 6 the lines labeled b_1, b_2, . . . b_{16} are the bits in the binary representation of the desired shift. At each block 62-69 the input is either multiplied by M^j or not multiplied depending on whether the corresponding gating bit b is 1 or zero, respectively. For example, to shift the current sequence contained in SRG 60 by 13 steps into the future, bits b_1 -b_{16} would be set as follows: b_1 =1, b_2 =0, b_4 =1, b_8 =1, b_{16} =0" (emphasis added); and shifting the PN code first phase with each of the phase-shifting mask (figures 6-9 column 8 line 11 to column 10 line 23. The have to use each of the shifting masks because the final shift is obtained only using all the masks selected to produce the shift. Stark specifically discloses in column 10 lines 52-61 "memory means for storing combining information that corresponds to pre-determined sleep intervals; means for extracting particular combining information from said memory means in response to said control information; and means for applying said combining information to selectively combine elements of said extracted current operating state using combinatorial logic to determine said new operating state" (emphasis added), and also in column 8 lines 11-54 "If only one shift or

multiples of it are needed, then the matrix is fixed and the corresponding combining logic can be used without the need for a matrix input, as shown in FIG. 4. The example in FIG. 4 provides a fixed shift of ten steps. However, circuitry for a shift having an arbitrary number of steps may also be beneficial, e.g., to compensate for awaking after different duration sleep periods. In order to calculate an arbitrary shift, an arbitrary power of M needs to be computed. If N is the length of the shift register sequence, e.g., N=31, any power of M up to 30 can be computed by multiplying some of the following: $M\ M^2\ M^4\ M^8\ M^{16}$ For example, to obtain M^{10}, $M^8 * M^2$ is calculated. If a particular shift of the nominal sequence is currently being used and an additional shift is desired, then multiplying the current M by another power of M will provide a new shift. This can be accomplished using mod-N arithmetic of the two shifts to obtain a new binary representation of the desired shift. To obtain different shifts requires different connections in the combining logic. An arbitrary shift can be obtained by having five different shifting operations that are either gated on or off as shown in FIG. 6. Therein, shift register generator 60 holds the current or "old" sequence state. The first circuit 62 forms a shift of this sequence by one clock cycle. The second circuit 64 takes the output of circuit 62 and shifts it by two clock cycles. The third circuit 66 shifts the output of circuit 64 by four clock cycles. The fourth circuit 68 shifts the output of circuit 66 by 8 clock cycles and the last stage 69 shifts the output of circuit 68 by 16 cycles. By selectively gating each of these circuits, i.e., to either include their contribution or not, an arbitrary shift is obtained. In FIG. 6 the lines labeled $b_1, b_2, \ldots b_{16}$ are the bits in the binary representation of the desired shift. At each block 62-69 the input is either

multiplied by M^j or not multiplied depending on whether the corresponding gating bit b is 1 or zero, respectively. For example, to shift the current sequence contained in SRG 60 by 13 steps into the future, bits b_1 -b_{16} would be set as follows: b_1 =1, b_2 =0, b_4 =1, b_8 =1, b_{16} =0" (emphasis added)). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 2, Easton and Stark disclose claim 1, Easton also discloses a method for determining a first time interval that includes accepting a first time interval from among a plurality of first time intervals (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64; the first time interval is the time reference provided by the searcher 205). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract). Therefore, it would have been obvious to combine Easton and Stark to obtain the invention as specified in claim 2.

As per claim 4, Easton and Stark disclose claim 1, Easton also discloses a method further comprising generating the PN code at a first chip period (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64); and accepting a second time interval proportionally related to the first chip period (figure 1 block 203, the second time interval is the programmed sleep interval, column 4 lines 37-64; and column 5 lines 12-42).

As per claim 5, Easton and Stark disclose claim 4, Easton also discloses a method for accepting a plurality of second time intervals (figure 1 block 203, the second time interval is the programmed sleep interval, column 4 lines 37-64; and column 5 lines 12-42. Easton discloses that the sleep interval could be a multiple of the slot duration 80 ms).

As per claim 6, Easton and Stark disclose claim 5, Stark also discloses a method for determining a first time interval from among a plurality of first time intervals that are offset from each other by predetermined periods of time (figure 6; column 8 line 11 to column 10 line 23. The masks are shifting 1, 2, 4, 8, and 16 time periods corresponding to 00001, 00010, 00100, 01000 and 10000). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 7, Easton and Stark disclose claim 6, Stark also discloses that the PN code has $(2^N - 1)$ states with a period m= $(2^N - 1)$ time the first chip period (column 1 lines 21-40); selecting a first time interval in the range between zero and m, with a resolution of x (figures 6-9 column 8 line 11 to column 10 line 23.); and generating a PN code with a second phase that is offset with respect to time in units of x (figures 6-9 column 8 line 11 to column 10 line 23. The final shift is obtained only using all the masks selected to produce the shift). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 8, Easton and Stark disclose claim 7, Stark also discloses that x is the first chip period (column 8 lines 11-54). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 9, Easton and Stark disclose claim 7, Stark also discloses that x is equal to the first chip period times q, where q is an integer (column 10 lines 3-14). Easton and Stark are analogous art because they are from the same field of endeavor.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 11, Easton and Stark disclose claim 7, Stark also discloses a direct sequence spread spectrum (DSSS) receiver (column 1 lines 11-20) with a memory is included (figures 3c and 4; column 8 lines 8-10), determining a first time interval in the range between x and nx (column 8 lines 11-31); storing n phase-shifting masks in memory, corresponding to the plurality of first time periods between x and nx (figures 6-9 column 8 lines 11-67; column 10 lines 52-53; column 11 lines 18-19); and selecting a phase-shifting mask from the n phase-shifting masks stored the memory (figures 6-9 column 8 lines 11-67; column 10 lines 54-57; column 11 lines 18-19). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 12, Easton and Stark disclose claim 7, Stark also discloses a direct sequence spread spectrum (DSSS) receiver (column 1 lines 11-20) with the memory is included (figures 3c and 4; column 8 lines 8-10), determining a first time interval in the

range between x and nx (column 8 lines 11-31); storing $\log_2$ (n) phase-shifting masks in memory corresponding to $\log_2$ (n) intermediate time intervals between x and nx (figures 6-9 column 8 lines 11-67; column 10 lines 52-53; column 11 lines 18-19); summing intermediate first time intervals to form a first time interval sum (figures 6-9 column 8 lines 11-67); where selecting a plurality of phase-shifting masks includes selecting phase-shifting masks from memory corresponding to each of the intermediate time intervals in the first time interval sum (figures 6-9 column 8 lines 11-67; column 10 lines 54-57; column 11 lines 18-19); and where shifting the PN code first phase with phase-shifting mask includes shifting the PN code first phase with the phase-shifting masks selected from memory (figures 6-9 column 8 lines 11-67; column 10 lines 58-60). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 13, Easton and Stark disclose claim 1, Stark also discloses that the plurality of phase-shifting masks are selected from a number of stored phase-shifting masks, and the number of stored phase-shifting masks is adjustable (figures 6-9 column 8 line 11 to column 10 line 23). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by

Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 14, Easton and Stark disclose claim 11, Easton also discloses synchronizing the accepted transmissions with the generated PN code (figure 3 slot n column 6 lines 22-42; figure 4A blocks 400-414 column 7 line 65 to column 8 line 11); following the selecting of a second time interval, powering-off the first chip rate clock during a slotted mode sleep interval (figure 3 power down column 6 lines 22-42; figure 4A blocks 438-440 column 8 lines 23-29); powering-on the first chip rate clock (figure 3 after sleep column 6 lines 22-42; figure 4A blocks 442-460 column 8 lines 23-64); and wherein determining the first time interval includes determining the sleep time interval that the first rate clock was powered-off (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64; the first time interval is the time reference provided by the searcher 205); and following the generating of the PN code with the second phase, resynchronizing the generated PN code with the accepted transmissions (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64).

As per claim 23, Stark discloses claim 18, Stark doesn't disclose a first chip rate clock having an output connected to the PN code generator, the first chip rate clock being powered-off at the beginning of the first time period, and being powered-on at the finish of the first time period; and a searcher section having an input connected to PN code generator output to accept the PN code with the second phase shift, the searcher

section resynchronizing the accepted transmissions with the generated PN code, following the power-on of the first chip rate clock. Easton discloses a first chip rate clock having an output connected to the PN code generator, the first chip rate clock being powered-off at the beginning of the first time period, and being powered-on at the finish of the first time period (figure 3 slot n column 6 lines 22-42; figure 4A blocks 432A-446 column 7 line 65 to column 8 line 11); and a searcher section having an input connected to PN code generator output to accept the PN code with the second phase shift, the searcher section resynchronizing the accepted transmissions with the generated PN code, following the power-on of the first chip rate clock (abstract, column 2 line 51 to column 3 line 33; summary of the invention; figure 1 block 205 column 4 lines 38-45). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 24, Easton and Stark disclose claim 23, Easton also discloses the application means accepts a second time interval corresponding to a slotted sleep mode interval (figure 1 block 203, the second time interval is the programmed sleep interval, column 4 lines 37-64; and column 5 lines 12-42. Easton discloses that the sleep interval could be a multiple of the slot duration 80 ms), where the application means programs the PN code generator to be powered off for the second time interval

(figure 3 asleep period slot n column 6 lines 22-42; figure 4A blocks 432A-446 column 7 line 65 to column 8 line 11); and wherein the application means determines the first time interval in response the actual time that the PN code generator was powered-off (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64; the first time interval is the time reference provided by the searcher 205). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract).

As per claim 25, Easton discloses a method for conserving power in a slotted mode of operation comprising generating a synchronized pseudorandom noise (PN) code to despread transmissions (figure 3 slot n column 6 lines 22-42; figure 4A blocks 400-414 column 7 line 65 to column 8 line 11); accepting a slotted mode sleep second time interval from a plurality of second time intervals (figure 1 block 203, the second time interval is the programmed sleep interval, column 4 lines 37-64; and column 5 lines 12-42. Easton discloses that the sleep interval could be a multiple of the slot duration 80 ms); beginning the sleep mode at a first phase of the PN code (figure 3 power down column 6 lines 22-42; figure 4A blocks 438-440 column 8 lines 23-29); ending the sleep interval (figure 3 after sleep column 6 lines 22-42; figure 4A blocks 442-460 column 8 lines 23-64); determining the first time interval between the beginning and the end of the

sleep interval (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64; the first time interval is the time reference provided by the searcher 205); selecting a phase-shifting mask from storage in response to the first time interval (figure 1 block 207A-207N column 4 lines 53-56); offsetting the PN code first phase with the phase-shifting mask (figure 1 block 207A-207N column 4 lines 37-64; and column 8 lines 45-64 indicates how the shifting is done using the mask); generating the PN code with a second phase (abstract, column 2 line 66 to column 3 line 12; summary of the invention; figure 1 block 207A-207N column 4 lines 37-64); and resynchronizing the generated PN code to despread transmissions (figure 3 slot n column 6 lines 22-42; figure 4A blocks 400-414 column 7 line 65 to column 8 line 11). Easton doesn't disclose storing a plurality of phase-shifting masks in a memory at a first time; selecting a plurality of phase-shifting masks; and shifting the PN code first phase with each of the phase-shifting mask. Stark discloses storing a plurality of phase-shifting masks in a memory at a first time (column 10 lines 52-53; column 11 lines 23-24. Stark specifically discloses in column 10 lines 52-61 "memory means for storing combining information that corresponds to pre-determined sleep intervals; means for extracting particular combining information from said memory means in response to said control information; and means for applying said combining information to selectively combine elements of said extracted current operating state using combinatorial logic to determine said new operating state" (emphasis added), and also in column 8 lines 11-54 "If only one shift or multiples of it are needed, then the matrix is fixed and the corresponding combining logic can be used without the need for

a matrix input, as shown in FIG. 4. The example in FIG. 4 provides a fixed shift of ten steps. However, circuitry for a shift having an arbitrary number of steps may also be beneficial, e.g., to compensate for awaking after different duration sleep periods. In order to calculate an arbitrary shift, an arbitrary power of M needs to be computed. If N is the length of the shift register sequence, e.g., N=31, any power of M up to 30 can be computed by multiplying some of the following: M M^2 M^4 M^8 M^{16} For example, to obtain M^{10}, $M^8 * M^2$ is calculated. If a particular shift of the nominal sequence is currently being used and an additional shift is desired, then multiplying the current M by another power of M will provide a new shift. This can be accomplished using mod-N arithmetic of the two shifts to obtain a new binary representation of the desired shift. To obtain different shifts requires different connections in the combining logic. An arbitrary shift can be obtained by having five different shifting operations that are either gated on or off as shown in FIG. 6. Therein, shift register generator 60 holds the current or "old" sequence state. The first circuit 62 forms a shift of this sequence by one clock cycle. The second circuit 64 takes the output of circuit 62 and shifts it by two clock cycles. The third circuit 66 shifts the output of circuit 64 by four clock cycles. The fourth circuit 68 shifts the output of circuit 66 by 8 clock cycles and the last stage 69 shifts the output of circuit 68 by 16 cycles. By selectively gating each of these circuits, i.e., to either include their contribution or not, an arbitrary shift is obtained. In FIG. 6 the lines labeled b_1, b_2, . . . b_{16} are the bits in the binary representation of the desired shift. At each block 62-69 the input is either multiplied by M^j or not multiplied depending on whether the corresponding gating bit b is 1 or zero, respectively. For example, to shift the current sequence

contained in SRG 60 by 13 steps into the future, bits b_1 -b_{16} would be set as follows: b_1 =1, b_2 =0, b_4 =1, b_8 =1, b_{16} =0" (emphasis added)); selecting a plurality of phase-shifting masks and shifting the PN code first phase with each of the phase-shifting mask (figures 6-9 column 8 line 11 to column 10 line 23. The have to use each of the shifting masks because the final shift is obtained only using all the masks selected to produce the shift). Easton and Stark are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the method disclosed by Stark in the CDMA receiver disclosed by Easton. The suggestion/motivation for doing so would have been to properly advancing sequence states in conjunction with sleep mode without detrimentally draining battery capacity (Stark abstract). Therefore, it would have been obvious to combine Easton and Stark to obtain the invention as specified in claim 25.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
08-07-2006

TEMESGHEN GHEBRE... PRIMARY EXAMINER 9/14/06